SL622, Programmable Linear Hall Effect Sensor IC

Description

SL622 is the leading product of SENK SEMI.'s programmable Linear Hall IC. After programmed, it can measure the magnetic field which applied to the IC plane vertically and provide a voltage output that is proportional to the applied magnetic field. The customer can configure the sensitivity，quiescent (zero field) output voltage，reference voltage and temperature compensation coefficient through programming with the VIOUT pin on power-on condition. The configure parameters are programmed into the non-volatile memory so as to ensure the IC's stability in worse electrical and magnet environment.

It can be programmed to be ratio-metric or non-ratio-metric output with VCC. SL622 can be easily used to manufacture current transducers when working with the magnetic core. The factory can make different range of transducers through programming different sensitivity.

Besides，SL622 can be applied to be position sensor in the condition when the magnetic field change with the magnet position change.

Features

- Fantastic Wide Selectable sensitivity range from 1.14 to 230mV/G
- SL622-GLFB，VREF pin can be programmed to two different modes：input or output
- VREF Input mode：The reference voltage is selectable in the range of 0.5/0.75/1.5/2.5V.
- VREF Output mode：The quiescent (zero field) output voltage can be programmed into two modes:

  Ratio-metric：0.5Vcc （Supports all SL622 series）

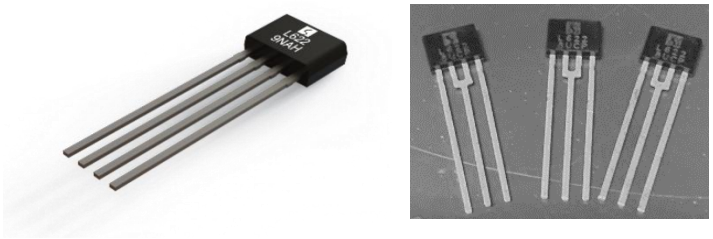
  Ratio-metric：0.1Vcc （Supports SL622-A3FB and SL622-GLFB series）

  Non-ratio-metric：fixed 2.5V （Supports all SL622 series）
- The quiescent error of VIOUT – VREF can be adjusted to be < ±4mV@2.5v
- The Sensitivity error after programmable< ±6mV@3.3V /5V
- High current load ability，VIOUT & VREF can be connected to differential output mode
- Faster Response time <2us
- Single supply +3.3 V/ 5V
- Independent intellectual Property Rights

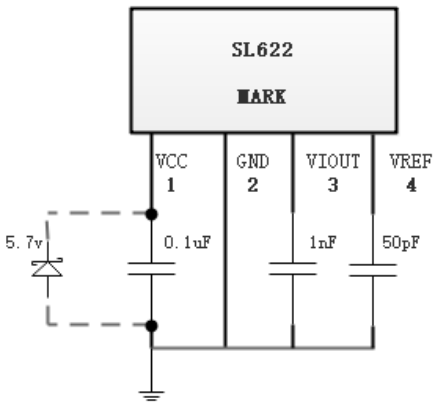
Package View

Top view

T094 TO94-3



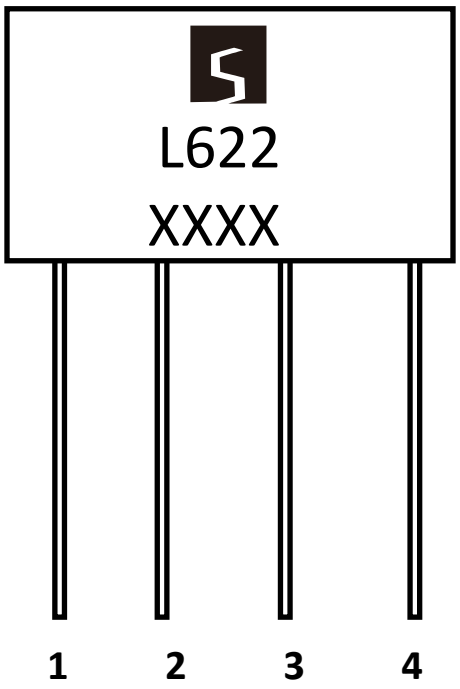
Typical Application

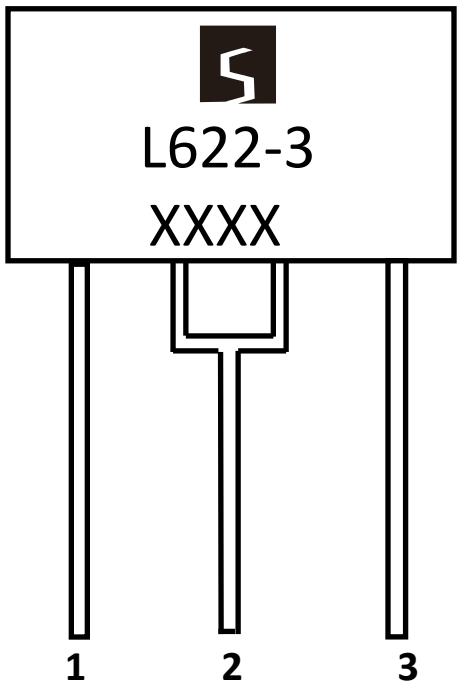


Order information

Part Number	Power Supply	Special Code	Packaging	Temp Range	Packing	Selection guide
SL622-BEFB	5V	B	E (TO94)	F(-40~125℃)	B(1k/Bag)	Not for new design （Vref Low Drive）
SL622-A3FB	3.3/5V	A	(3) TO94-3			New package:1.9mm pinch
SL622-GLFB	5V	G	L (TO94)			High speed and high drive capacity with VREF

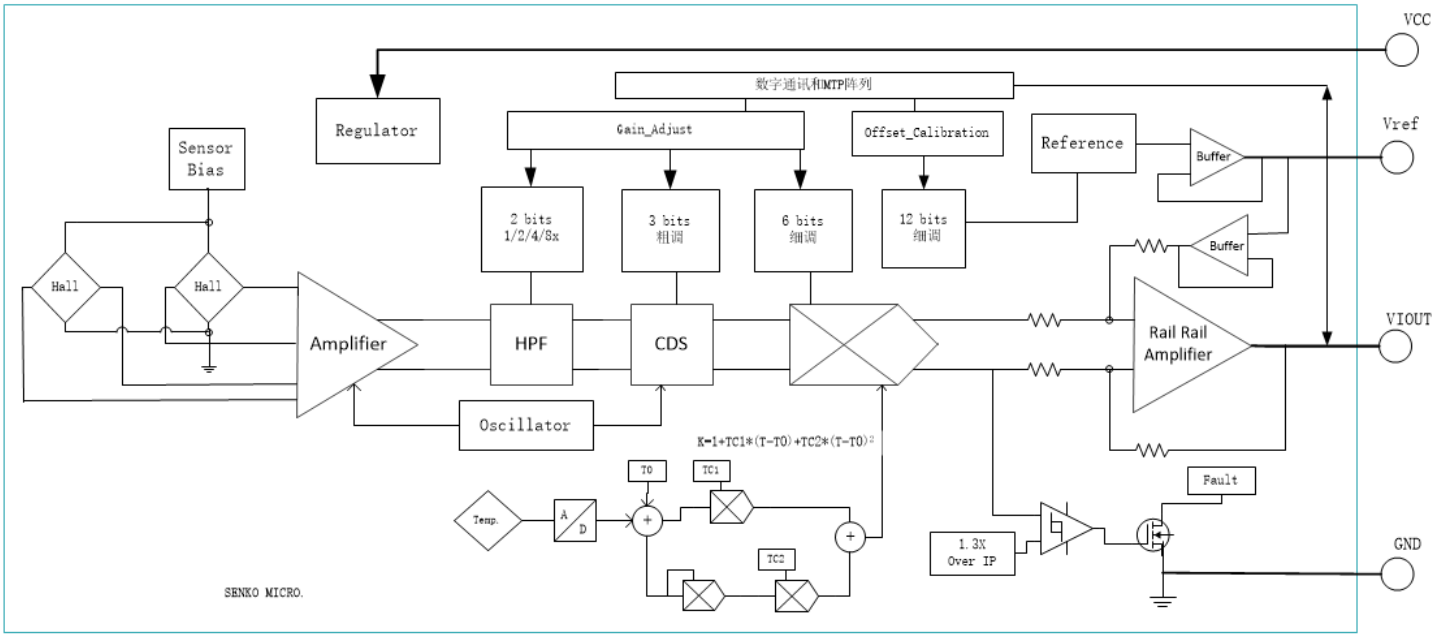
Pin Configuration（top view）





Pin number	Pin Name	Description
1	VCC	Device power supply terminal
2	GND	Signal Ground terminal
3	VIOUT	Analog output signal, also should be used to programming digital I/O
4	VREF	SL622-GLFB： 1. Reference terminal Also support differential output mode with VIOUT 2. VREF pin can be programmed to peripheral input voltage (0.5/0.75/1.5/2V) range

Functional Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

Characteristic	Symbol	Notes	Rating	Unit
V_{CC}	Supply voltage		6.0	V
V_{RCC}	Reverse Supply Voltage		-0.1	V
VOUT	Output voltage		6.0	V
V_{RIOUT}	Reverse Output Voltage		-0.1	V
T_A	Nominal Operating Ambient Temperature		-40~125	℃
$T_{J\ (max)}$	Maximum Junction Temperature		165	℃
T_{stg}	Storage Temperature		–65~170	℃
$I_{REF\ Source\ Current}$	Vref Current Sour	Vref shorted to GND.	3.47	mA
$I_{REF\ Sink\ Current}$	Vref Current Sink	Vref shorted to VCC	40	mA
$I_{OUT(Source)}$	Output Current Source	Shorted Output-to-Ground Current	3.43	mA
$I_{OUT(Sink)}$	Output Current Sink	Shorted Output-to-VCC Current	40	mA
ESD	HBM mode		4	KV
V_{CC}	Supply voltage		6.0	V

Parameters of peripheral components

Device	Test Condition	Min	Typ	Max	Units
CVCC	Power filter capacitor, connected between V_{CC} / GND	--	0.1	--	uF
CVIOUT	Output VIOUT filter capacitor, connected between VIOUT / GND	--	1	1.5	nF
CVREF	VREF filter capacitor at reference end, connected between VREF / GND	--	50	100	pF

Common operating Characteristics

Note: Over full range of T_A=-40° C ~ 125° C, C_{Bypass}=0.1uF， C_{Load}=1nF, unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage	V_{CC}	Programmed to be 5.0v(SL622 full series)	4.5	5.0	5.5	V
		Programmed to be 3.3v(SL622-A3FB)	3.0	3.3	3.6	V
Supply Current	I_{CC}	V_{CC} = 5.0V, output open	10	20	26	mA
		V_{CC} = 3.3V, output open	10	13	16	mA
Output Load Capacitance	CL	VOUT to Gnd		1	1.5	nF
Output Load Resistance	RL	VOUT to Gnd	2.2			kΩ
VREF Load Capacitance	CLREF	VREF to Gnd		50	100	pF
VREF Load Resistance	RLREF	VREF to Gnd，SL622-BEFB	300			kΩ
		VREF to Gnd，SL622-GLFB	2.2			kΩ
Nonlinearity	ELIN	Measured using full-scale and half-scale IP			1	%
Response Time	t_r	T_A = 25°C, C_{OUT} =1nf			2.5	μS
Response delay time	T_{pd}	IP= Full scale		1.2		uS
Power-On Time	t_{PO}	Output reaches steady state level，T_J = 25°C		100	200	uS
Chopping Frequency	Fc	T_A = 25°C		1		MHz
Frequency Bandwidth	f	Small signal -3 Db, CL=1 nF SL622-A3FB		80		kHz
		Small signal –3 dB, CL= 1 nF SL622-GLFB		170		kHz
		Small signal –3 dB, CL= 1 nF SL622-BEFB		120		kHz

Output characteristic after programmable

Note: Over full range of T_A=-40°C ~ 125°C, C_{Bypass}=0.1uf， C_{Load}=1nF, V_{CC}=5V,Based on ferrite， unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Quiescent Output Voltage	VOUT (QU)	Non variable ratio， T_A = 25°C,V_{CC}=5V	2.495	2.5	2.505	V
		Variable ratio, T_A = 25°C, VCC=3.3/5V		0.5*Vcc		V
		Variable ratio, T_A = 25°C, VCC=3.3/5V		0.1*Vcc		V
		V_{REF} is the input mode， SL622-GLFB T_A = 25°C , V_{CC}=5V		0.5/0.75/1.5/ 2.5		V
Electrical offset voltage @ IP = 0	V_{OE}	VOUT - V_{REF} @ V_{REF}= 2.5v,TA=25℃	-5	-	5	mV
Sensitivity change ratio	Sen_coef	Variable ratio: V_{REF}@0.5*V_{CC} V_{CC}=4.5v~5.5v Sens_coef=Sens(VCC)/Sens(5V)		V_{CC}/5		
VOUT linear rail to rail output range	Vrail-rail	R_L=4.7kΩ	10		90	%VCC
V_{REF} Voltage Output Temperature Error	$V_{REF-ERROR}$	TA = 25℃	-5		5	mV
		TA = -40°C to 25℃	-30		30	mV
		TA = 25°C to 125℃	-25		25	mV
Quiescent Voltage Output Temperature Error	VOUT-ERROR	TA = 25℃	-5		5	mV
		TA = -40°C to 25℃	-20		20	mV
		TA = 25°C to 125℃	-30		30	mV
Total Output Error	E_{TOT}	T_A=25°C, output filtered	-1.2		1.2	%
		TA = -40°C to 25℃	-3		3	%
		TA = 25°C to 125℃	-5		5	%
Noise	V_N	TA = 25°C, COUT = 1nF, Sens=5mv/GS		120		mVp-p
		TA = 25°C, COUT = 1nF, Sens=5mv/GS		22		mVRMS
		TA = 25°C, COUT = Open, Sens=5mv/GS		122		mVp-p
		TA = 25°C, COUT = Open, Sens=5mv/GS		21		mVRMS

Accuracy characteristic curve

Figure 1: VREF Voltage vs. Temperature

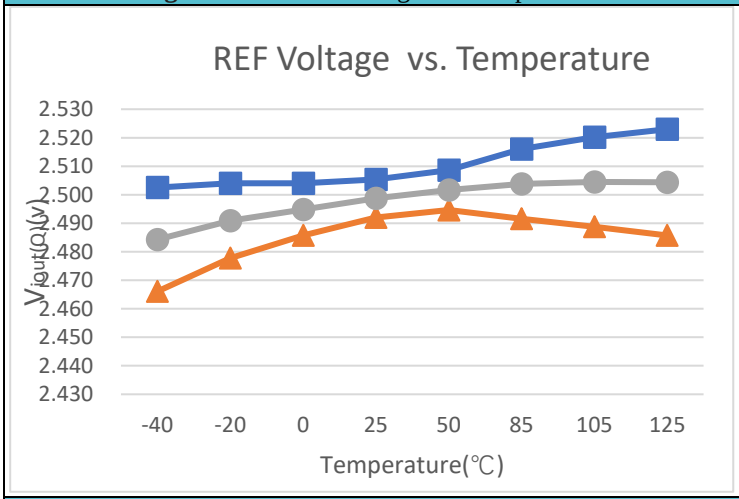


Figure 2: VREF Error vs. Temperature

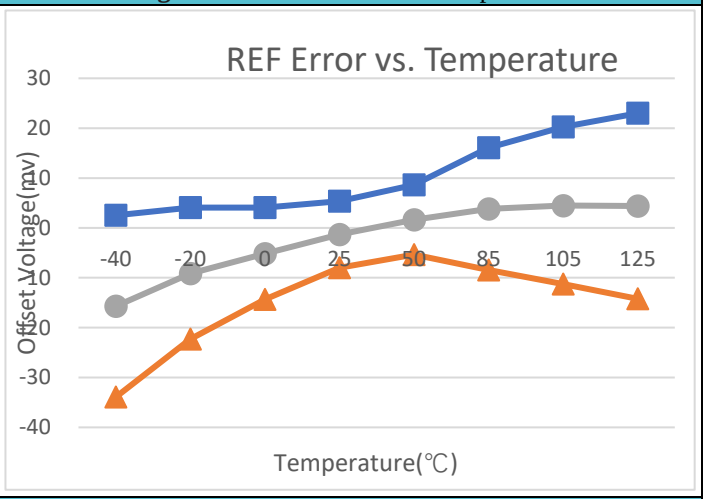


Figure 3: Nonlinearity vs. Temperature

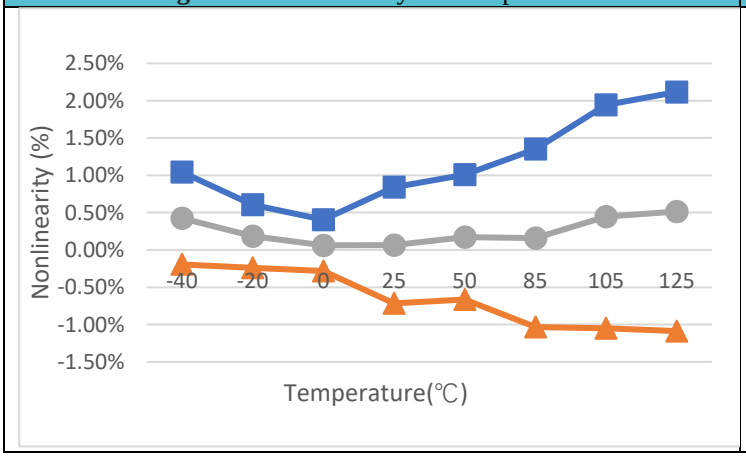
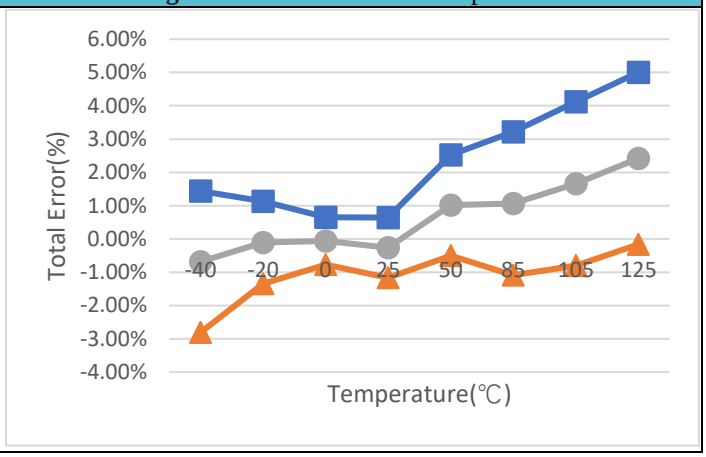


Figure 4: Total error Vs Temperature



AC characteristic diagram

Figure 1: Rise Time

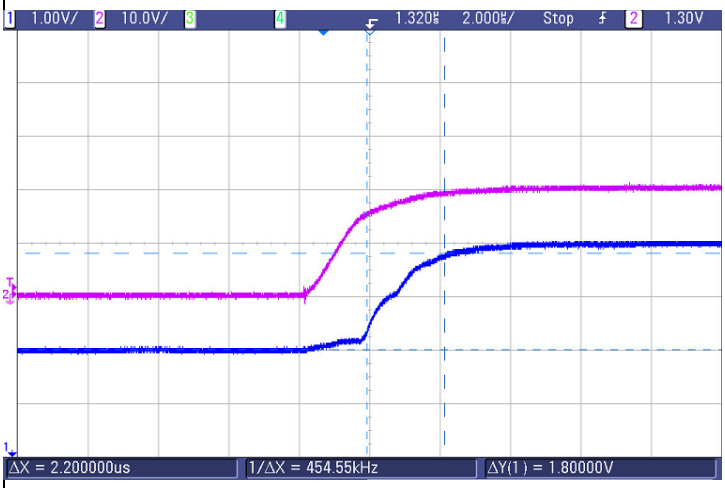


Figure 2: Response Time

Figure 3: Propagation Delay

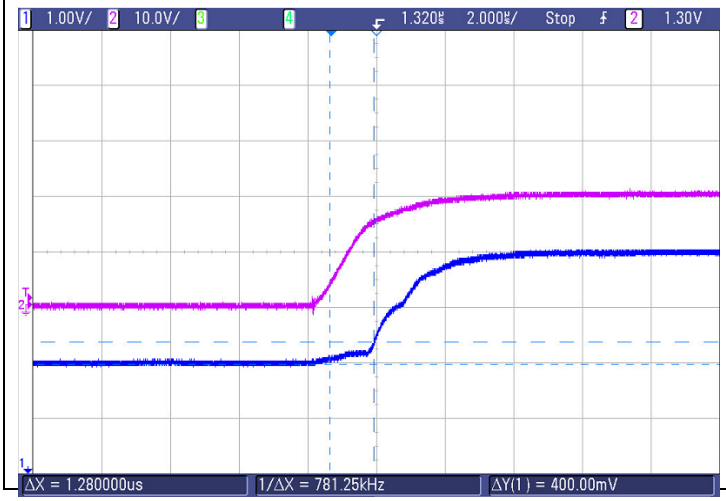


Figure 4: Noise spectrum

Dynamic characteristic curve

Figure 1: Sinewave transient response

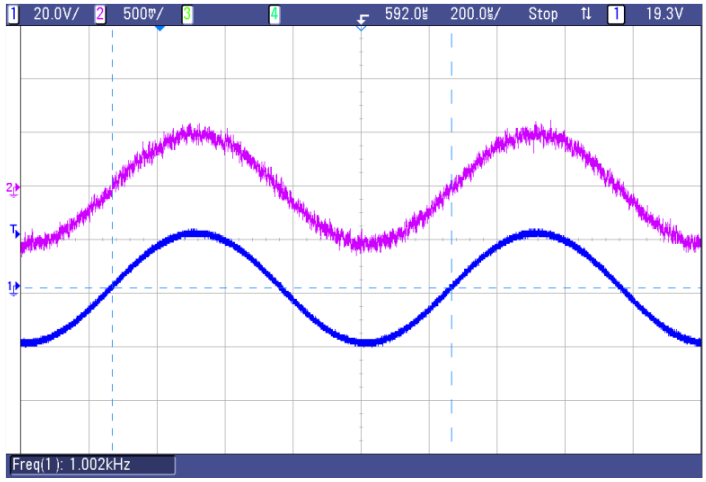


Figure 2: Impulse transient response diagram

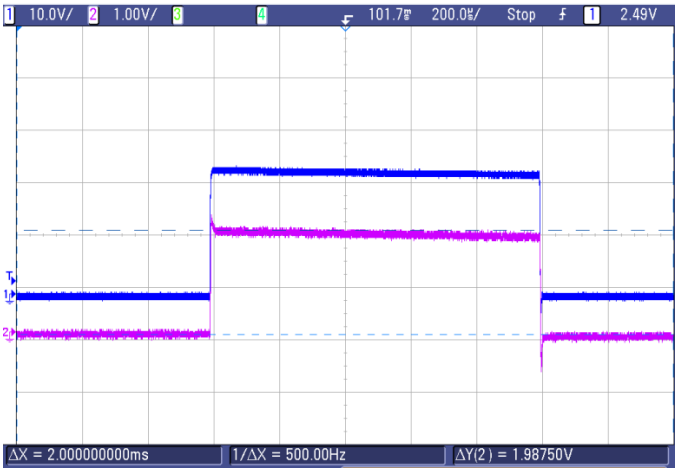
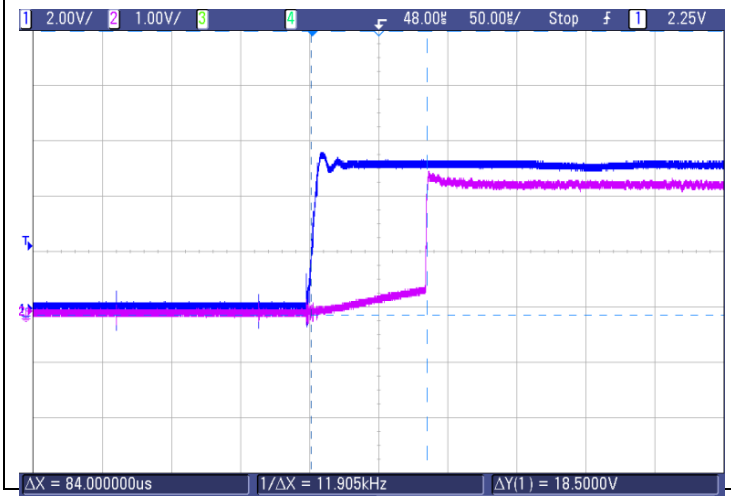


Figure 3: Power-On Time



Sensitivity programming bit

Symbol	Test Conditions		Min	Typ	Max	Unit
sel_sensor[1]	Readable by customer		-	1	-	Bit
INC_HALL_I	Readable by customer		-	2	-	Bit
S3_OUT_DRV	Readable by customer		-	1	-	Bit
S2_double	Readable by customer		-	1	-	Bit
Gain_COARSE	Readable by customer		-	2	-	Bit
Gain_FINE			-	9	-	Bit

sel_sensor[1]	INC_HALL_I	S3_OUT_DRV	S2_double	Gain_COARSE				
0	2	0	0	0	1.140	-	2.752	mv/Gs
0	0	0	0	0	1.710	-	4.128	mv/Gs
0	0	0	0	1	3.421	-	8.257	mv/Gs
0	0	0	0	2	6.842	-	16.514	mv/Gs
0	0	0	0	3	13.685	-	33.028	mv/Gs
0	0	0	1	3	27.371	-	66.056	mv/Gs
0	0	1	1	3	41.0568	-	99.084	mv/Gs
1	1	1	1	3	95.799	-	231.196	mv/Gs

Offset programming bit

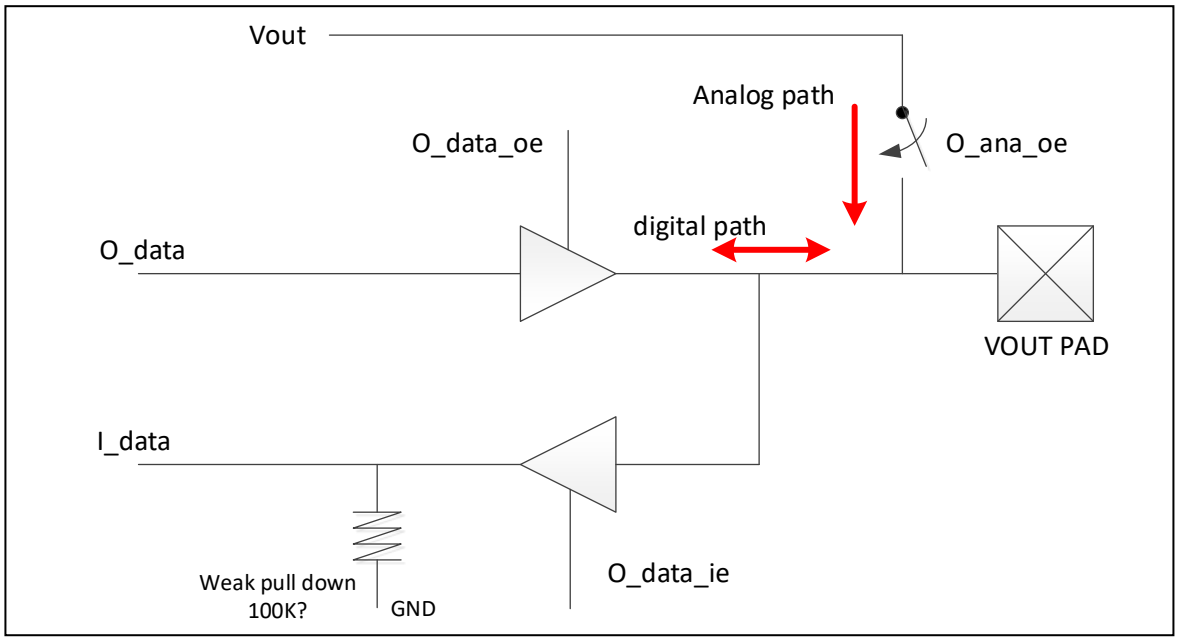
Characteristic	Symbol	Test Condition	Min	Typ	Max	Units
VREF Offset coarse programming Bits	VREF		-	6	-	Bit
		VREF output voltage (0 Gauss) adjustment	-250	-	250	mV
		Step adjustment		8		mV
VIOUT Offset fine tuning programming Bit	VIOUT			7		Bit
		VIOUT output voltage (0 Gauss) adjustment	-250	-	250	mV
		Step adjustment		4		mV

Non calibration programming bit

Characteristic	Symbol	Test Condition	Min	Typ	Max	Units
Working mode （Special Code : G）	VREF		-	2	-	Bit
		select output voltage 2b00: VREF=0.5*VDD, 2b01: VREF=2.5V, 2b10: VREF=0.1*VDD, 2b11: VREF from external	-	-	-	-
Select temperature coefficient	TC1			4		Bit
		select the sensitivity TC slope for temp 4b0000: 0ppm …… …… 4b1111:1280ppm	0	-	1280	ppm
		80ppm Step adjustment		80		ppm
Select temperature coefficient	TC2			4		Bit
		select the sensitivity TC slope for temp 4b0000: 0ppm …… …… 4b1111:1280ppm	0	-	1280	ppm
		80ppm Step adjustment		80		ppm
Select the breakpoint of the two stage TC calibration	TCTH			2		Bit
		2b00: -20℃ 2b01: -10℃ 2b10: 0℃ 2b11: 65℃	-	-	-	-
Magnetic reversal				1		Bit
		Reverse induction 1b0: default 1b1: opposite polarity	-	-	-	-

Programming description

- As a programming pin, VIOUT supports input or output communication, which is digital input and programmable mode by default
- through lock protocol, the function of VIOUT is switched to one-way analog output mode, and digital input is no longer supported.
- Through the ability of analog multi driver, read the digital code in the analog state, turn off the analog output, switch to the analog mode, realize the analog entering the digital mode, and solve the secondary programming.



Feature reference application

◆ SL622-GLFB Application of VREF

VREF is equal to static output value
The relationship between VIOUT and VREF: VIOUT=B*SENS+VREF （B：flux magnetic）

◆ SL622 VREF function selection

Characteristic	Symbol	Test Condition	Min	Typ	Max	Units
Working mode	VREF		-	2	-	Bit
		select output voltage 2b00: VREF=0.5*VDD, 2b01: VREF=2.5V， 2b10: VREF=0.1*VDD， 2b11: VREF from external	-	-	-	-

- Select VREF=0.5 * VDD, output voltage and Vcc as a ratio relationship, supporting all SL622 series
- Select VREF=0.1 * VDD, output voltage and Vcc as a ratio relationship, suitable for SL622-A3FB, SL622-GLFB
- Select VREF=2.5V, output voltage and Vcc as non proportional relationships, applicable to all SL622 series
- When selecting VREF external drive, VREF is an input mode that supports external input voltage. The static output voltage can be modified to 0.5/0.75V and 2/2.5V; Sensitivity remains unchanged, suitable for SL622-GLFB

◆ Delay time t_{PD} and response time $t_{response}$

Propagation Delay (t_{pd})

The time interval between a) when the applied magnetic field reaches 20% of its final value, and b) when the output reaches 20% of its final value

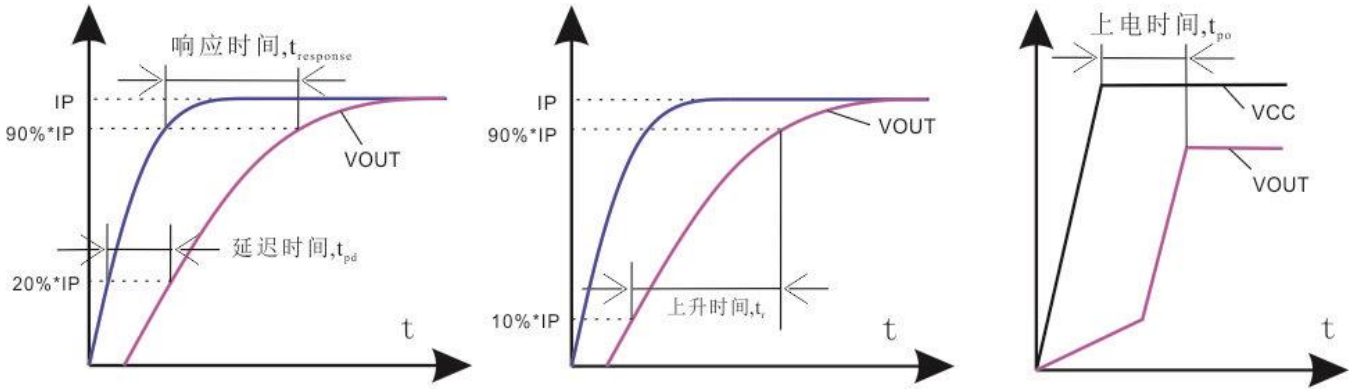
Response Time ($t_{RESPONSE}$)

The time interval between a) when the applied magnetic field reaches 90% of its final value, and b) when the sensor reaches 90% of its output corresponding to the applied magnetic field . The parameter is also shown in the Electrical Characteristics table and in the performance data table.

Rise Time (t_r)

The time interval between a) when the sensor IC reaches 10% of its final value, and b) when it reaches 90% of its final value Power-On Time (t_{PO})

Power on time is used to describe the time difference between the secondary side and the power supply VCC, that is, the time difference between the secondary side output and the VCC when it reaches the steady-state output value.

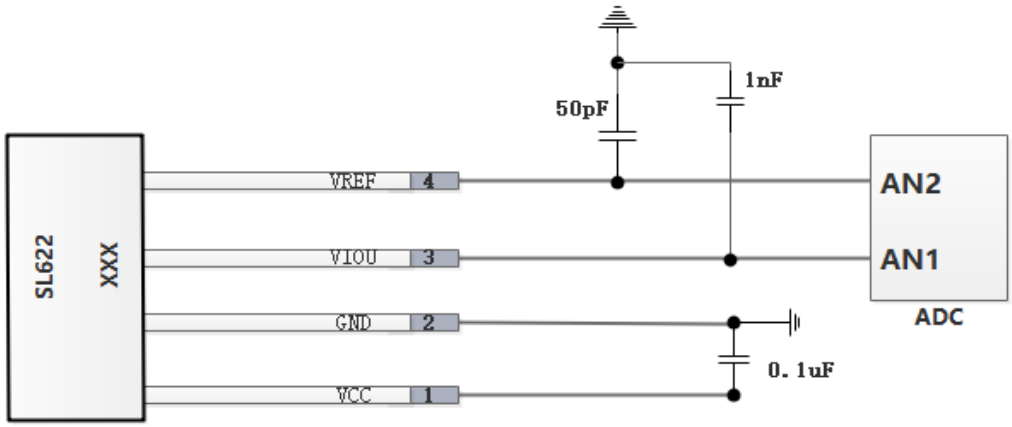


Application circuit diagram

Support AC or DC

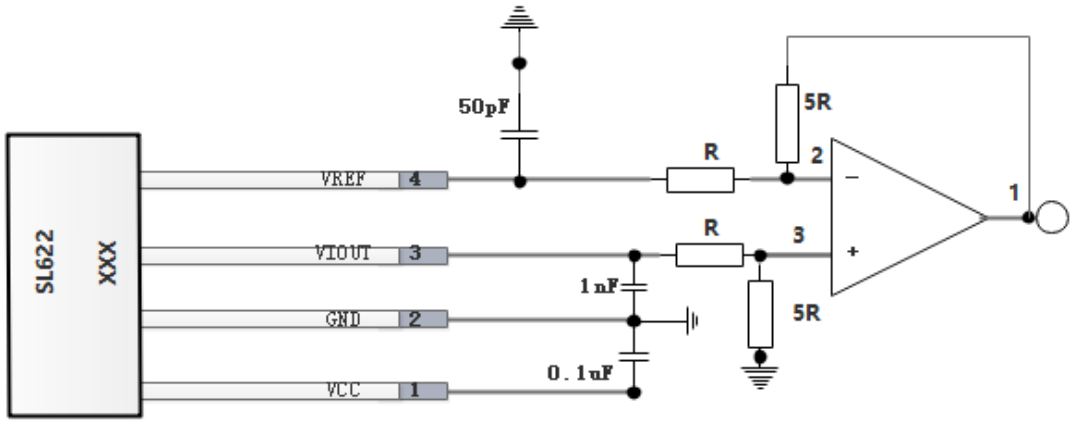
1) SL622 and ADC connection diagram

VREF is the output terminal when selecting 0.5*Vcc 、0.1*Vcc、2.5V function.

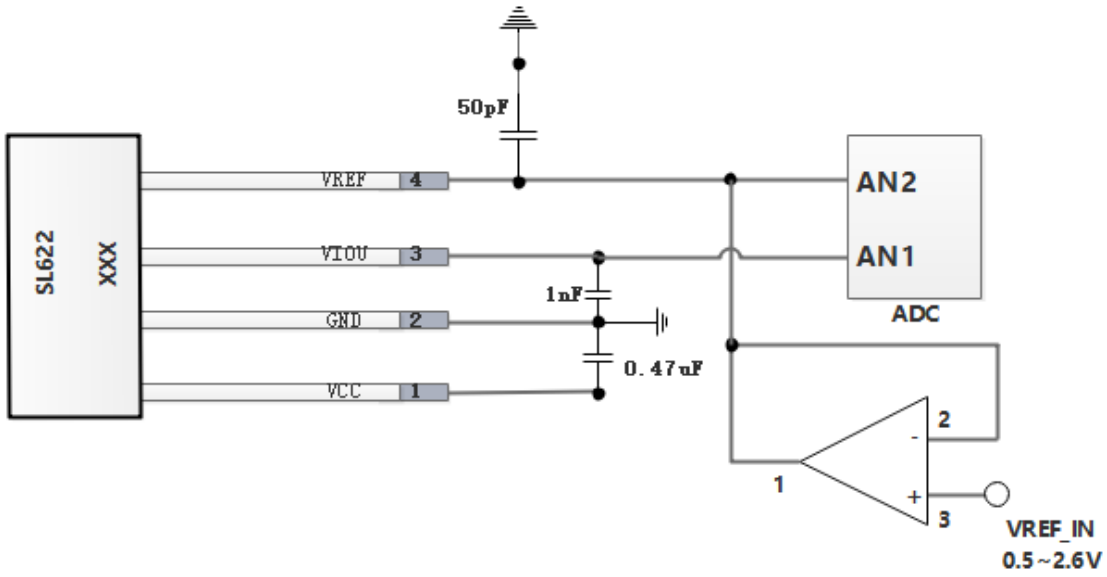


2) Schematic diagram of differential mode between VIOUT and VREF of SL622-GLFB :

Pictured : VIOUT = IP * Sensitivity * （5R / R）

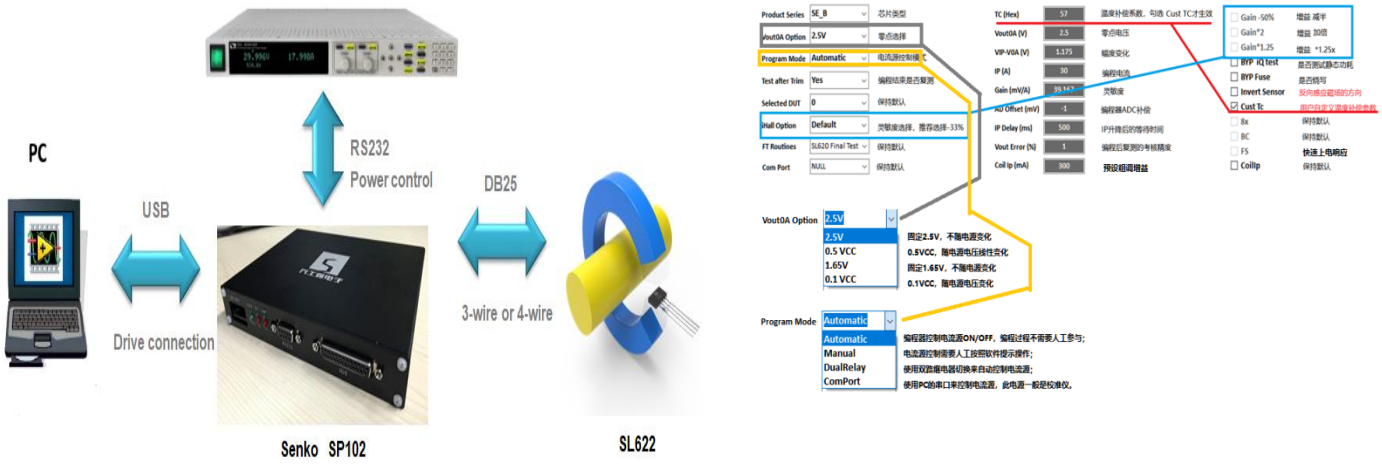


3) When VREF is selected as the input terminal, VREF voltage can be modified to 0.5/1V and 2/2.5V,and VIOUT static voltage is equal to VREF voltage (SL622-GLFB)



Programming System

The SL622 incorporates a serial interface that allows an external controller called SP102 to automatically calibrate in the MTPROM. Please contact with FAE of SENK SEMI.
Email: fae@senkomicro.com



calibration system

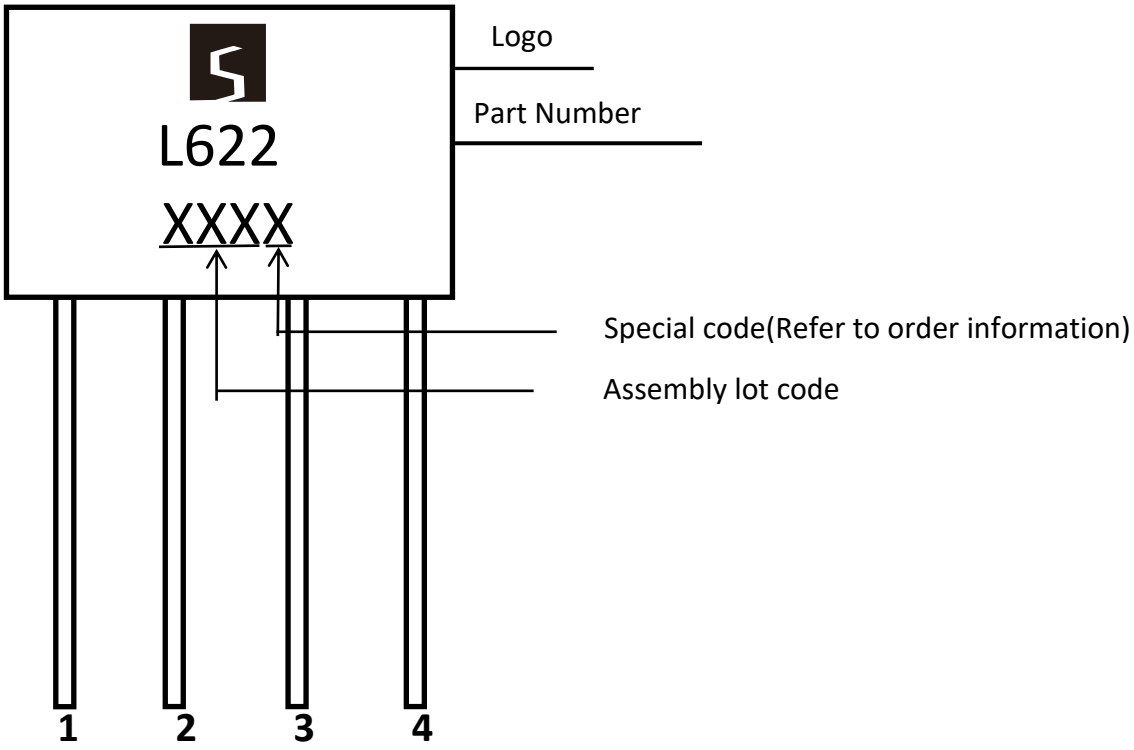
- The programming hardware takes SP102 as the core, the USB serial port installation driver realizes the PC connection, and the RS232 serial port transmission command realizes the control current source; the DB25 serial port provides high-precision 5V power supply for the IC, and the VIOUT as the programming pin realizes the communication transmission.

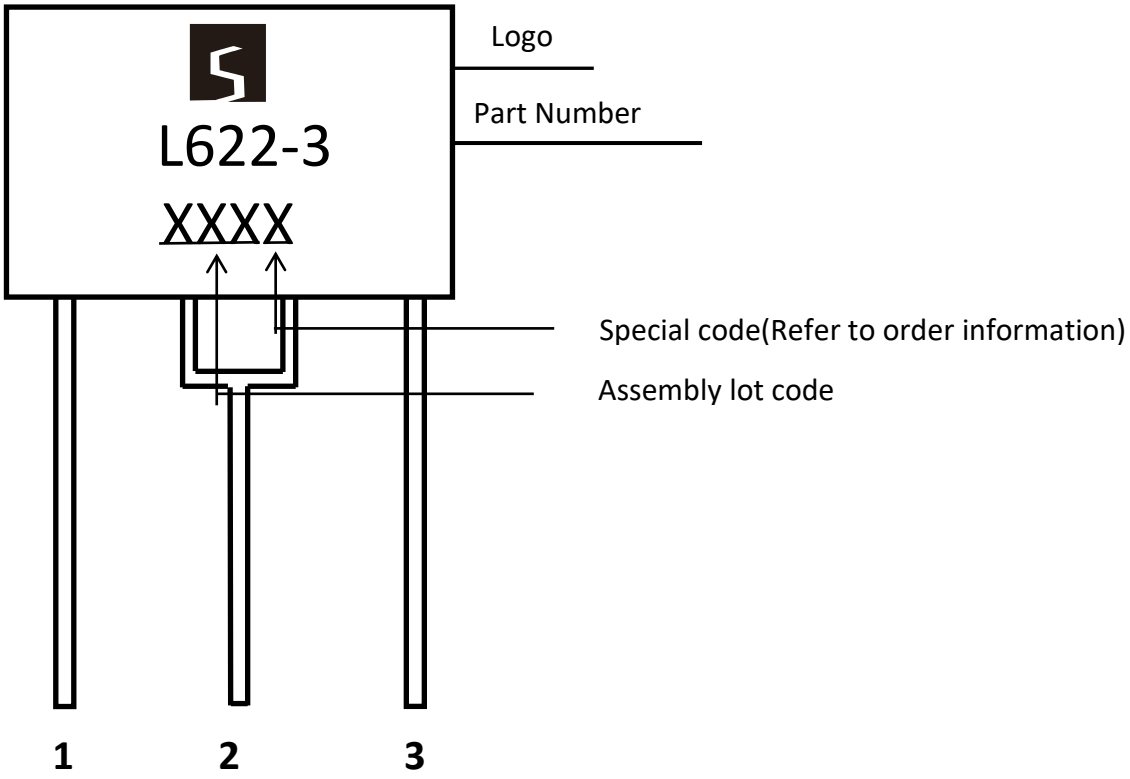
- The program system opens all programmable functions, supports users to program in a wide range of sensitivity, and has greater flexibility.

- There are error proofing measures in the program settings. For example, Bin3 and bin4 product programs have prompt functions. The product program is unlocked by default, that is, the product can be reprogrammed and calibrated repeatedly to reduce the error probability.

◆ Note: please refer to the technical application manual for details of programming calibration.

◆ Mark Description

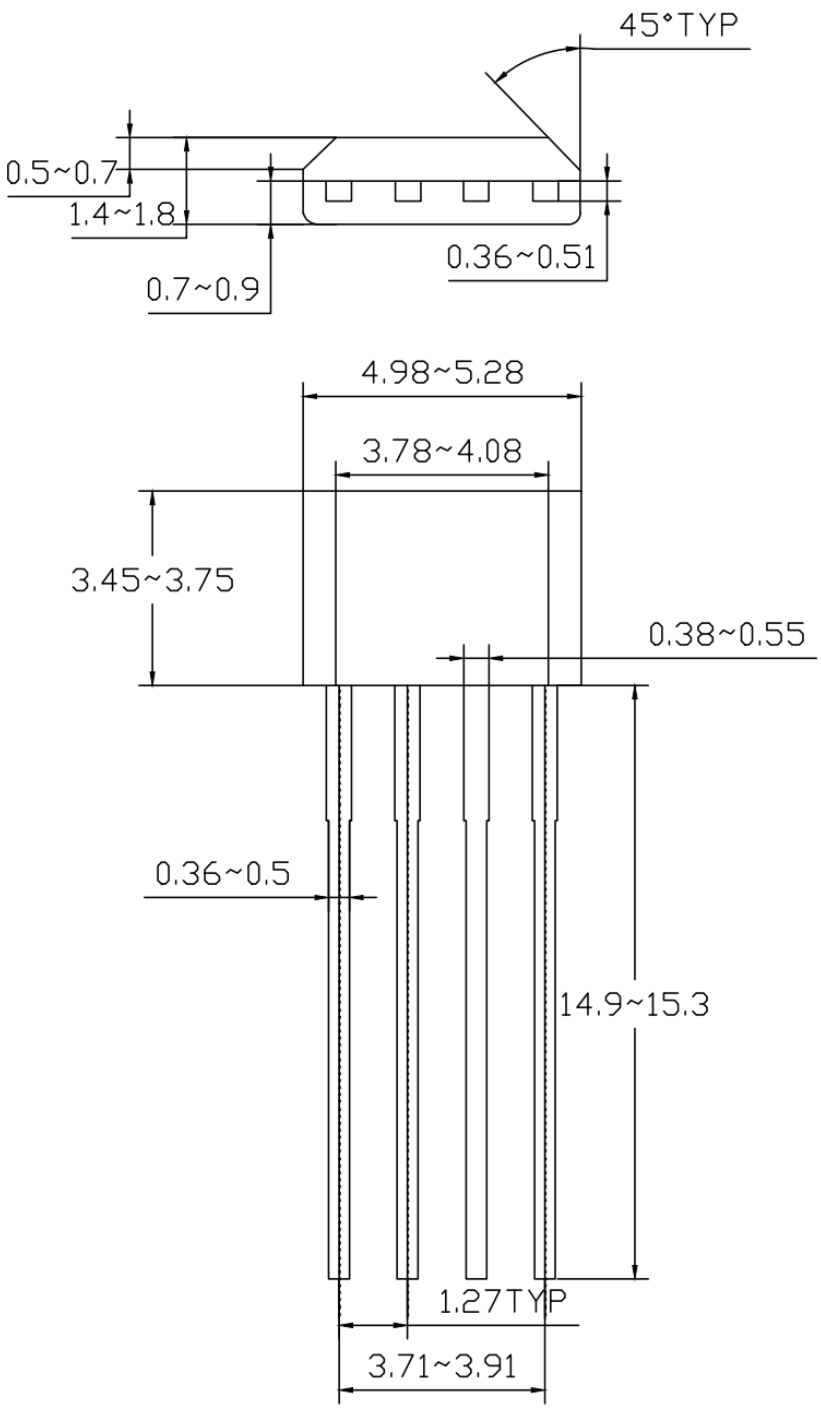




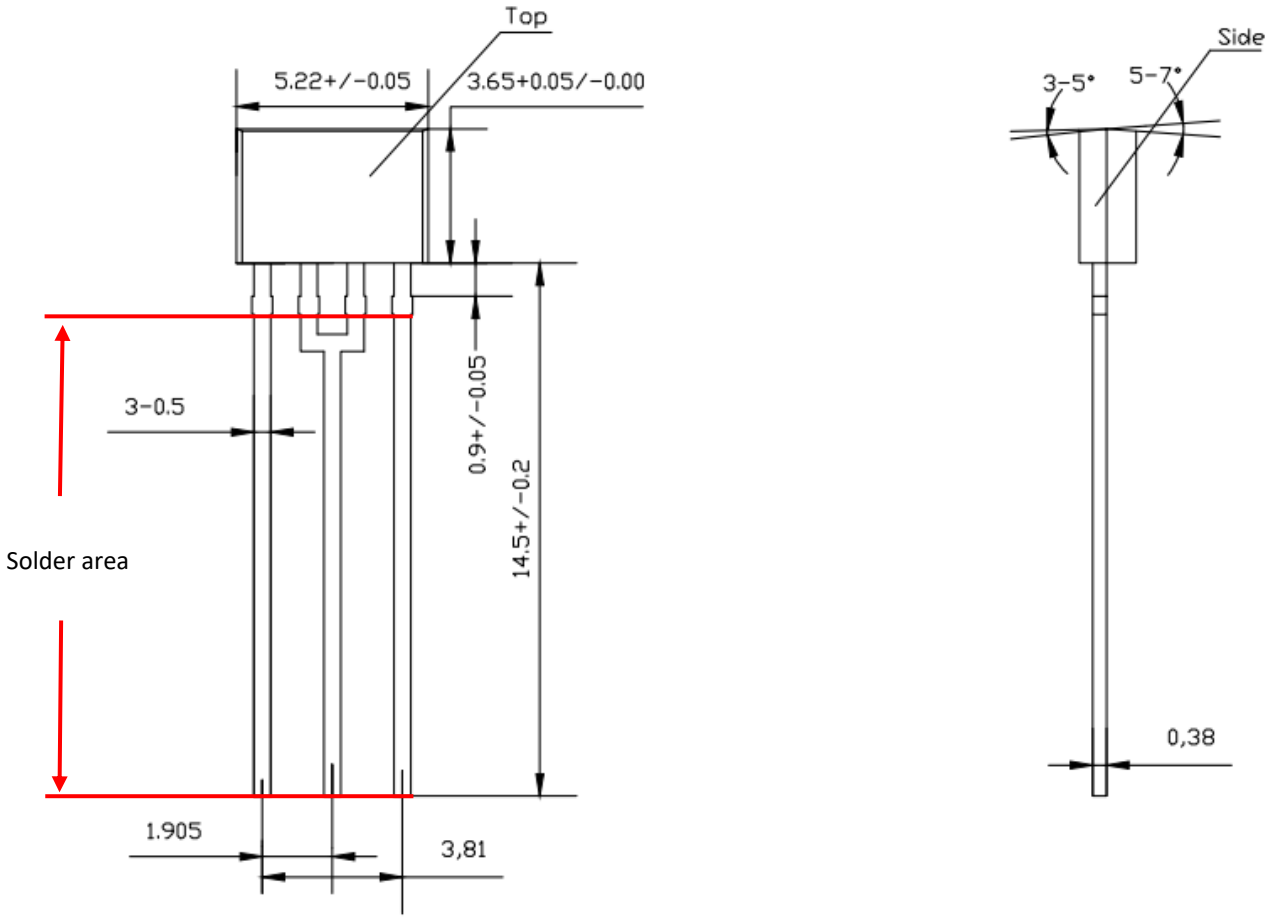
Package Information

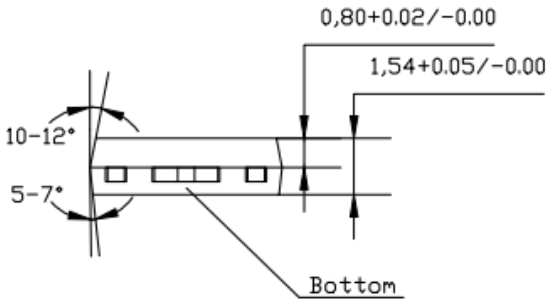
Note: all dimensions are in millimeters.

SL622-BEFB

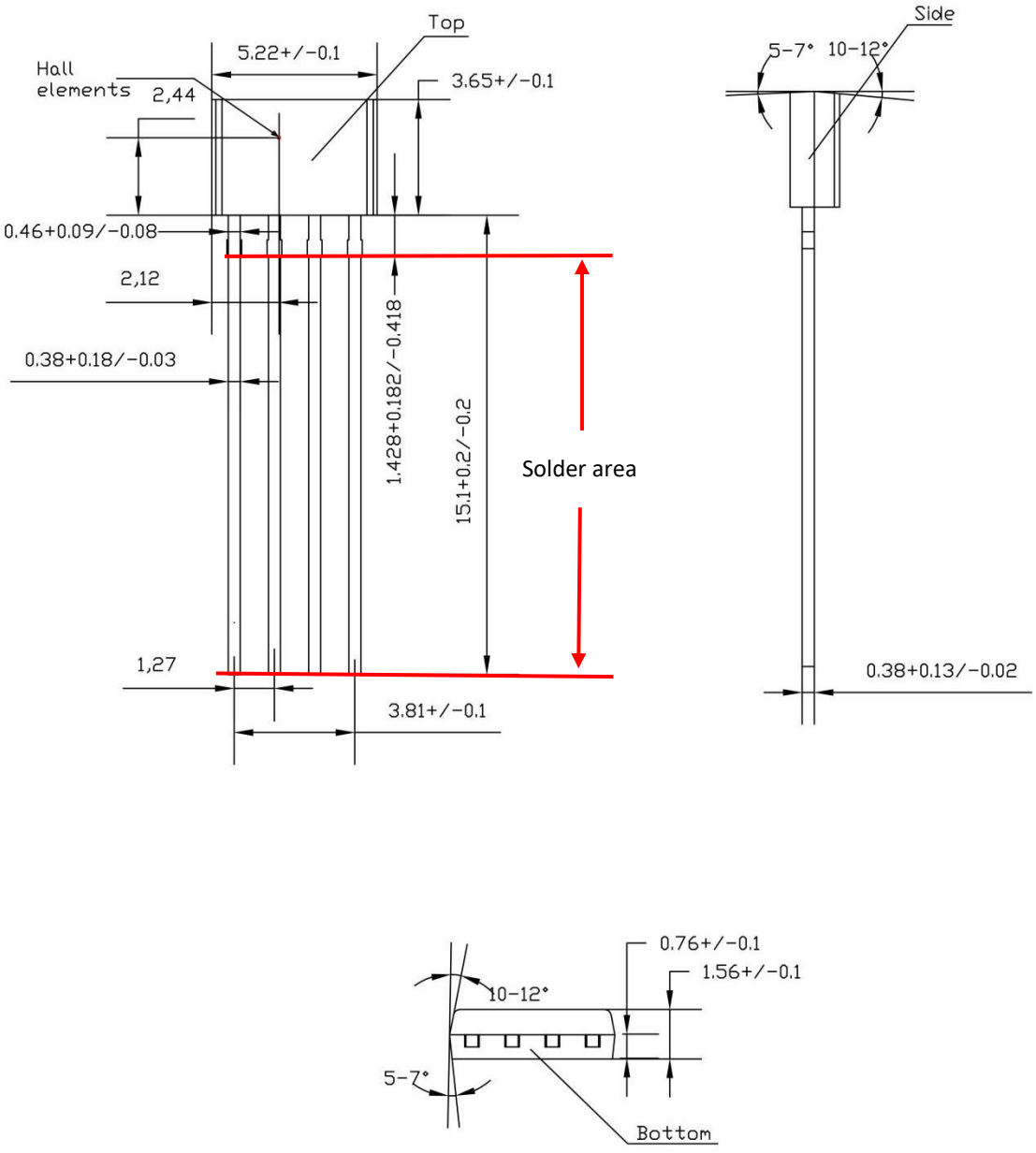


SL622-A3FB



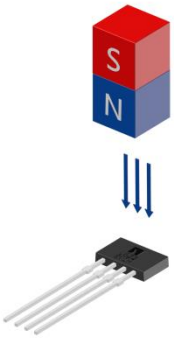


SL622-GLFB


Top
Side
Hall
elements
2,44
5.22+/−0.1
3.65+/−0.1
5−7°
10−12°
0.46+0.09/−0.08
2,12
0.38+0.18/−0.03
1.428+0.182/−0.418
15.1+0.2/−0.2
Solder area
1,27
3.81+/−0.1
0.38+0.13/−0.02
0.76+/−0.1
1.56+/−0.1
10−12°
5−7°
Bottom

Magnetic induction direction selection

Characteristic	Symbol	Test Condition	Min	Typ	Max	Units
Magnetic reversal	-			1		Bit
		Reverse induction 1b0: default 1b1: opposite polarity	-	-	-	-



Note:

- By default, when the N-pole magnetic field is close to the identification surface of sl622, the voltage output will rise accordingly.
- When {opposite polarity} is selected, when the magnetic field is S-pole close to the SL622 identification surface, the voltage output will rise accordingly.

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Revision Table

Revision	Change	Page	Author	Date
1.0	Initial draft based XG601		Deng	2019.02
2.0	Add SL622-GL Version; Update Hall's position in the chip; Add Vref Info. In Page 6;Check and updated POD in page 17; Modify the packaging information of TO94 Modify working mode;Update marking information; Update SL622-BEFB POD information; Add solder area; Update information;		MWJ	2024.07.17